WHAT IS CLAIMED IS:

1. A back illuminated photodiode array comprising:

a first conductive type semiconductor substrate having a light-incident surface and an opposite surface with a plurality of recessed portions located opposite said light-incident surface; and

a plurality of second conductive type semiconductor regions spatially detached at each bottom of said recessed portions; wherein said semiconductor regions individually constitute pn junctions together with said semiconductor substrate.

2. A back illuminated photodiode array according to claim 1,

wherein said semiconductor substrate regions between a plurality of said recessed portions constitute a frame part which is thicker than said recessed portions.

3. A back illuminated photodiode array according to claim 1,

wherein said semiconductor substrate is composed of a single semiconductor substrate.

4. A back illuminated photodiode array according to claim 1,

wherein said semiconductor substrate is provided with a first semiconductor substrate having said light-incident surface and

a second semiconductor substrate bonded to said first

semiconductor substrate and having side walls of said recessed portions.

5. A back illuminated photodiode array according to claim 4, further comprising an etching stop layer existing between said first semiconductor substrate and said second semiconductor substrate and having resistance to a specific etching agent to be used for said second semiconductor substrate.

6. A back illuminated photodiode array according to claim 4, further comprising an insulation layer existing between said first semiconductor substrate and said second semiconductor substrate.

7. A back illuminated photodiode array according to claim 2, comprising a plurality of electrode pads formed on each top surface of said frame part and individually and electrically connected to said semiconductor regions.

8. A back illuminated photodiode array according to claim 7, further comprising:

an electric insulation layer formed on said frame part; and

a conductive member formed on said electric insulation layer and connecting electrically said semiconductor regions with said electrode pads.

9. A back illuminated photodiode array according to claim 8, wherein said electric insulation layer is provided with a contact hole for connecting an end of said conductive

member to said semiconductor regions.

10. A back illuminated photodiode array according to claim 2, wherein said semiconductor regions extend from said bottoms to side surfaces of said recessed portions.

11. A back illuminated photodiode array according to claim 2, wherein said semiconductor regions extend from said bottoms over side surfaces of said recessed portions to a top surface of said frame part.

12. A back illuminated photodiode array according to claim 11, comprising:

an electric insulation layer formed on said frame part and having a contact hole opposing said top surface; and electrode pads electrically connected to said semiconductor regions through said contact hole.

13. A back illuminated photodiode array according to claim 2, wherein said frame part is provided with a first conductive type separation region higher in impurity concentration than said semiconductor substrate.

14. A back illuminated photodiode array according to claim 1 wherein an opening size of said recessed portions decreases with an increase in the depth of said recessed portions.

15. A back illuminated photodiode array according to claim 1, wherein said light-incident surface side of said semiconductor substrate is provided with a first conductive type accumulation layer which is higher in impurity

concentration than said semiconductor substrate.

16. A back illuminated photodiode array according to claim 4, wherein mutually opposing surfaces of said first semiconductor substrate and said second semiconductor substrate are different in their crystal plane orientation.

17. A semiconductor device, comprising:

a back illuminated photodiode array according to claim 7; and

a wiring board supporting said back illuminated photodiode array,

wherein said wiring board is electrically connected to said back illuminated photodiode array through said electrode pads.

18. A semiconductor device according to claim 17, comprising a scintillator placed on said light-incident surface of said semiconductor substrate.

19. A semiconductor device according to claim 17, wherein resin or air is filled in a space between said wiring board and said opposite surface of said semiconductor substrate.

20. A manufacturing method for the back illuminated photodiode array according to claim 4, said manufacturing method comprising a step of bonding said second semiconductor substrate to said first semiconductor substrate.

21. A manufacturing method for the back illuminated photodiode array according to claim 20, the manufacturing

method comprising a recessed portion forming step of forming a recessed portion by etching for forming a recessed portion corresponding region on said opposite surface of said second semiconductor substrate.

22. A manufacturing method for the back illuminated photodiode array according to claim 21, wherein the etching at said recessed portion forming step is carried out until an etching stop layer or an insulation layer existing between said first semiconductor substrate and said second semiconductor substrate is exposed.

23. A manufacturing method for the back illuminated photodiode array according to claim 21, wherein mutually opposing surfaces of said first semiconductor substrate and said second semiconductor substrate are different in their crystal plane orientation and the etching at said recessed portion forming step is carried out until at least the opposite surface of said first semiconductor substrate is exposed.

24. A manufacturing method for the back illuminated photodiode array according to claim 21,

wherein a step for forming said semiconductor region is provided with either

a post addition step in which, after said recessed portion forming step, impurities are doped to the bottoms of said recessed portions to form said semiconductor regions or

a previous addition step in which, before said recessed portion forming step, impurities are previously doped to the opposite surface of said first semiconductor substrate.

25. A manufacturing method for the back illuminated photodiode array according to claim 15, further comprising a step for forming said accumulation layer higher in impurity concentration than said semiconductor substrate on said light-incident surface side.